REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1, 4-8 and 12-14 are presently active in this case. Claims 2-3 and 9-10 were cancelled by a previous amendment. The present Amendment amends independent Claims 8, and 12-13 without introducing any new matter; and cancels Claims 11 and 15 without prejudice or disclaimer.

The outstanding Office Action rejected Claims 1, 4-8, and 12-13 under 35 U.S.C. § 103(a) as unpatentable over Arai et al. (U.S. Patent No. 5,457,473, hereinafter "Arai") in view of Nakano et al. (Japanese Patent Application No. JP 2000-250526, hereinafter "Nakano"). Dependent Claims 11 and 14-15 were indicated as allowable if rewritten in independent form.

Applicants acknowledge with appreciation the indication of allowable subject matter. In response, independent Claim 8 is amended to recite all the features of dependent Claim 11, and independent Claims 12-13 are amended to recite all the features of dependent Claim 15. Consequently, dependent Claims 11 and 15 are cancelled without prejudice or disclaimer. No new matter has been added. Moreover, Applicants respectfully submit that because the pending Office Action has considered the features of dependent Claims 11 and 15, these amendments also do not raise any questions of new issues that would require further search and/or consideration by the Examiner.

In response to the rejection of independent Claims 1 and 7 under 35 U.S.C. § 103(a), Applicants respectfully request reconsideration of these rejections and traverse the rejections, as discussed next.

Briefly summarizing, Applicants' independent Claim 1 is directed to an image processing apparatus that executes predetermined signal processing on an input signal and

outputs an image signal generated to driving unit of a display apparatus. The apparatus includes a superposing unit for superposing control data for controlling the driving unit on a vertical blanking data segment of the image signal, ***the control data being composed of a plurality of data elements, each data element being composed of a data byte that is repeated multiple times with each clock signal of the image processing apparatus to generate a repetitive data element series for each data element***; and outputting unit for outputting the image signal with the control data superposed thereon to the driving unit, wherein the control data is provided for control parameters of the display apparatus that is to be controlled by the driving unit.

Turning now to the applied references, Arai is directed to an image display apparatus 1b capable of adjusting a display picture by an input unit. (Arai, Abstract, ll. 1-3, Fig. 1.) A control signal Sc having control data C_D to adjust the display picture is added to a video signal RGB or a synchronization signal Hs and Vs that is produced by a control signal addition circuit 16 located in a computer body 1a, and is sent to the display apparatus 1b. (Id., Abstract, ll. 3-10, Fig. 1, col. 4, ll. 57-65.) The display apparatus 1b includes a control signal separation circuit 18 that can extract the sent control data C_D from the control signal Sc. (Id. from col. 4, l. 66, to col. 5, l. 6, and col. 5, ll. 29-45.) Arai explains that the control data C_D is added to either the R, B, G, H_s or V_s signal, as control data between a start bit and a stop bit. (Arai, col. 6, ll. 9-13, Fig. 3) Moreover, Arai explains that the control data is generated in sync with the horizontal synchronizing signal Hs. (Arai, col. 5, ll. 60-67.)

However, and as confirmed by the pending Office Action, Arai fails to teach that the control data is composed of a plurality of data elements, each data element being composed of a data byte that is repeated multiple times with each clock signal of the image processing apparatus, as required by Applicants' independent Claim 1. (March 30, 2009 Office Action, p. 3, ll. 2-6.) But the Office Action has rejected these features by pointing out to the

reference Nakano at paragraphs [0017]-[0022], and by asserting that the combination between Arai and Nakano is proper. (Office Action, p. 3, ll. 7-15.) Applicants respectfully disagree, as next discussed.

The applied reference Nakano is directed to a system that can transmit image data to a display device 200 together with command data set that is sent two times to the display device 200, in case of a transmission error. (Nakano, ¶ [0007], Fig. 1.) Nakano explains that the command data set is send twice in series to the receiver section 206 of display device 200, in synchronization with a clock signal and a synchronization signal. (Nakano, ¶ [0017], Fig. 3.) Nakano explains that an interface cable 11, used to send data to the differential receiver 22 of the receiver section 206, can be used to send a 24-bit data signal. (Nakano, ¶ [0018], Fig. 2, "data 23".) Nakano uses a latch 31 and a EXOR circuit 41, to check whether there is an error between two timely-adjacent 24-bit words that were transmitted, to detect an error in transmission. (Nakano, ¶¶ [0020]-[0021], Fig. 2.) In other words, Nakano transmits two identical data words having 24 bits. (Nakano, Fig. 3). However, Nakano fails to teach that a plurality of data elements, *each data element* being composed of a data byte that is repeated multiple times with each clock signal of the image processing apparatus, as required by Applicants' independent Claim 1. In other words, as shown in a non-limiting embodiment of Applicants' Figure 5, data elements W_0, W_1, W_2, . . . W_7 are sent, where each of the data elements W_0, W_1, W_2, . . . W_7 are composed of a byte that is repeated. (Applicants' Fig. 5, Specification, ¶¶ [0064]-[0065]). Nakano does not teach such a feature, because he merely sends two 24-bit data words twice, by repeating the entire 24-bit data set.

Therefore, even if the combination of Arai and Nakano is assumed to be proper, the cited passages of the combination fails to teach every element of Applicants' independent Claims 1 and 7. Accordingly, Applicants respectfully traverse, and request reconsideration of this rejection based on these references.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1, 4-8, and 12-14 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,

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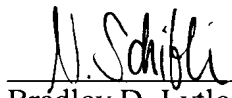

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